REMARKS

STATUS OF CLAIMS

Claims 1-36 are pending.

Claims 1 and 33-36 are rejected under 35 USC 112, 2nd paragraph, for indefiniteness, as indicated on page 2 of the Office Action.

The Examiner maintains, from the previous Office Action, rejection of claims 1-34, as being anticipated under 35 USC 102(e) by Ikegawa (US Patent No. 6,538,758).

Independent claim 35 and dependent claim 36 thereof are allowable if rewritten or amended to overcome the indefiniteness rejection.

Claims 1, 33, 35, and 36 are amended.

Thus, claims 1-36 remain pending for reconsideration, which is respectfully requested.

No new matter has been added in this Amendment.

35 USC 112, 2ND PARAGRAPH, REJECTIONS

Independent claim 1 is amended, taking into consideration the Examiner's comments on page 2 of the Office Action.

The Applicants assert that 35 USC 112, 2nd paragraph, concerning indefiniteness, specifies that the claims must particularly point out and distinctly define the metes and bounds of the subject matter that will be protected by the patent grant. More particularly, the definiteness standard is whether the scope of the claim is clear to a hypothetical person possessing the ordinary level of skill in the pertinent art. MPEP 2171 and 35 USC 112, 2nd paragraph.

The Applicants assert that claims 1, 33 and 35 are precise, clear, correct, and unambiguous, because the claims recite essential elements of the invention, and all of the recited essential structural elements/operations are clearly defined and expressly tied together/interrelated, as follows:

Claim 1 is drawn to an interface operating according to the present invention. Claim 1 recites,

> 1. (CURRENTLY AMENDED) An interface connectable to a host controller and an external bus, and that performs a predetermined bus reset sequence on the external ~~bus~~ bus, in response to a bus reset generated by a plug and play function according to a change in a status of the external bus, according to a process comprising:
>
> analyzing bus reset sequence data, including identification (ID) packet, provided from the external ~~bus~~bus, ***during*** the bus reset sequence ~~and~~,
>
> ***determining*** whether the bus reset sequence has been completed normally ***according to the analyzing*** of the bus reset sequence data, and
>
> ~~wherein the analysis circuit provides~~***providing the bus reset sequence data*** to the host controller when ~~determined that~~ ***according to the determining*** the bus reset sequence has been completed normally.

Therefore, independent claim 1 is definite, and withdrawal of the indefinites rejection is respectfully requested.

INDEPENDENT CLAIMS 33 AND 35

The Examiner in page 7 of the Office Action regarding the indefinites rejection, asserts "Applicants do not provide any reason as to why the amendment should overcome the rejections" for claims 33 and 35. Independent claims 33 and 35 are further amended for clarity, taking into consideration the Examiner's comments.

Also, in page 11 of the Office Action, the Examiner provides that independent claim 35 and dependent claim 36 thereof, would be allowable if rewritten or amended to overcome the indefiniteness rejection.

Claim 33 is drawn to a self-diagnosis method by an interface, according to the present invention. The self-diagnosis method of the interface as recited in independent claim 33, provides,

> 33. (CURRENTLY AMENDED) A method of self-diagnosis by an interface having a transmitting circuit and a receiving circuit that are communicably connectable to an external bus, and the interface performing a predetermined bus connection procedure to connect with the external bus, comprising:
>
> connecting the transmitting circuit and the receiving circuit to each other prior to ~~a~~ connecting with the external bus via the predetermined bus connection procedure by the interface to connect with the external bus;
>
> transferring data from the transmitting circuit to the receiving circuit;
>
> comparing ~~received~~ data received by the receiving circuit with the transferred data; and
>
> self-diagnosing the transmitting and the receiving circuits according to the comparing of the ~~received~~data transferred and the data received ~~transferred data~~ between the transmitting and the receiving circuits, respectively, of the interface.

Independent claim 33 is amended to clarify that the predetermined connection procedure is performed by the interface and is "a predetermined bus connection procedure to connect with the external bus." Therefore, independent claim 33 is drawn to an interface that performs "a predetermined bus connection procedure to connect with the external bus" and performs the present invention's self-diagnosis method. In other words, the claimed present invention's "self-diagnosis method" for the interface is provided in addition to the interface's existing "bus connection procedure to connect with the external bus" (i.e., connecting the transmitting circuit and the receiving circuit to each other ***prior to ~~a~~ connecting with the external bus*** via the predetermined bus connection procedure by the interface to connect with the external bus").

Support for the claim amendments can be found, for example, on page 27, lines 10-16 and FIGS. 15 and 16 of the present Application.

Regarding the Examiner's comment that in claim 33 "the received data" does not have clear antecedent basis, claim 33 has been amended to provided clear antecedent basis.

Therefore, independent claim 33 is definite.

INDEPENDENT CLAIM 35

Claim 35 is drawn to a self-diagnosis method by an interface, according to the present invention. The self-diagnosis method of the interface as recited in independent claim 35, provides,

> 35. (CURRENTLY AMENDED) A method of self-diagnosis by an interface having a transmitting circuit and a receiving circuit that are communicably connectable to an external bus, and the interface performing a predetermined bus connection procedure to connect with the external bus, comprising:
>
> connecting the transmitting circuit and the receiving circuit to each other prior to ~~a~~ connecting with the external bus via the predetermined bus connection procedure by the interface to connect with the external bus; and
>
> ~~testing as the self-diagnosis a direct current characteristic of the interface by~~ transferring test direct current signals between the connected transmitting circuit and the receiving circuit of the interface, to test, as the self-diagnosis, a direct current characteristic of the interface; and
>
> ~~testing as the self-diagnosis an alternating current characteristic of the interface by~~ transferring a test data signal whose waveform is same as ~~that of~~ data ~~used~~ to be transferred during an actual non-test data transfer over the external bus by the transmitting and receiving circuits of the interface on the external bus, to test, as the self-diagnosis, an alternating current characteristic of the interface.

The Examiner comments that the "data used during actual non-test data transfer" and its "waveform" have not been properly defined or recited positively in the claim. Independent claim 35 is amended to positively recite the transferring of test direct current signals and the transferring of a test data signal whose waveform is same as data to be transferred during an actual non-test data transfer.

Further, the claim recitation is precise, clear, correct and unambiguous to one skilled in the art concerning transferring a test data signal whose waveform is same as data to be transferred in a non-test data transfer. MPEP 2171 and 2173.02, which provide that the

definiteness standard is whether the threshold requirements for clarity and precision are met, and not whether more suitable language or mode of expression are available. Further, the failure to provide explicit antecedent basis for terms does not always render a claim indefinite. If the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite. MPEP 2173.05(e). In claim 35, there can be no dispute as to what is a test data transfer, "prior to a connecting with the external bus," whose waveform is same as data "to be transferred during an actual non-test data transfer over the external bus."

Therefore, independent claim 35 is definite. And it is understood that independent claim 35 and dependent claim 36 thereof are allowable, as indicated by the Examiner.

35 USC 102(e) REJECTION

The Examiner maintains, from the previous Office Action, rejection of claims 1-34, as being anticipated under 35 USC 102(e) by Ikegawa (US Patent No. 6,538,758).

INDEPENDENT CLAIMS 1, 2 AND 32

Regarding independent claims 1, 2 and 32, the Examiner in page 7 of the Office Action essentially asserts that the claims are overly broad. In particular, the Examiner, in page 9, lines 17-20, of the Office Action, asserts that IDs of the respective node connected to the 1394 bus must be analyzed ***during (emphasis added)*** bus reset according to the 1394 specification and the Examiner relies on Short Introduction into IEEE 1394, Bus Reset; and IEEE Standard 1394a. Therefore, the Examiner alleges that Ikegawa's 1394 I/F is similar to the claimed present invention's, "***analyzing bus reset sequence data, including identification (ID) packet***, provided from the external ~~bus~~bus, during the bus reset sequence, ~~and~~ determining whether the bus reset sequence has been ***completed normally according to the analyzing of the bus reset sequence data***, and ~~wherein the analysis circuit provides~~providing the bus reset sequence data to the host controller when ~~determined that~~according to the determining the bus reset sequence has been completed normally" (e.g., claim 1). In other words, the Examiner appears to allege that the claims are similar to the IEEE 1394 bus reset. Also, the Examiner is relying on Ikegawa, FIG. 7 (serial bus management 815 allegedly corresponding to the claimed present invention's "analysis circuit 26") and column 4, lines 48-55.

The Applicants clarify a difference between the functions of the port circuit 21, physical layer circuit 22 and link circuit 23 (FIG. 3 of the present Application), which are part of the IEEE 1394 standard and described in page 10 of the specification, and the analysis of the information by the analysis unit 26 of the claimed present invention, as follows. In other words, the

Examiner is asserting in page 9 of the Office Action, that the IEEE 1394 port circuit 21, physical circuit 22 and link circuit 23, must determine whether a completed reset is normal or without error before arbitration and subsequent data transfer as part of the IEEE 1394 operation. The Examiner asserts that otherwise, the network will have to be reset and until the reset is completed without error or "normally" data will not be able to transfer.

However, the IEEE 1394 standard as described in the Short Introduction into IEEE 1394 cited by the Examiner and as also discussed in page 1, line 22 to page 2, line 10 of the present application, fails to disclose or suggest the claimed present invention's "analysis circuit 26" performing "***analyzing bus reset sequence data, including identification (ID) packet***, provided from the external ~~bus~~bus, ***during*** the ***bus reset sequence***" (e.g., claim 1). In other words, in a conventional IEEE 1394 interface, ***during*** a bus reset, self ID packets, ***which are not data packets***, are stored in an internal buffer memory and simultaneously transferred to a microprocessor unit (MPU). Therefore, in a conventional IEEE 1394, the port circuit 21, physical layer circuit 22 and link circuit 23 (FIG. 3) do not perform any error checking and leave error checking to the MPU (page 2, lines 24-26 of the present Application). Therefore, in the conventional IEEE 1394, the MPU determines whether the self ID packet has an error, which might be correctable via another reset by the MPU, such that the previous erroneous self ID packet is unnecessarily transferred to the MPU (page 2, lines 26-32 of the present Application). The claimed present invention avoids such a circumstance by providing the analysis unit 26, as shown in FIG. 3, which does not transfer the self ID packet to the MPU in the event of an error, as shown in FIG. 8, operations 75, 77 and 78.

Ikegawa fails to disclose or suggest analyzing bus reset sequence data including ID packet ***DURING*** a bus reset sequence (claims 1-12 and 32). Rather, Ikegawa discloses performing data transfer after a bus reset sequence is completed. Furthermore, Ikegawa does not analyze ID packets, because Ikegawa fails to discuss what function the serial bus management 815 of FIG. 7 performs. Also, as explained in the IEEE standard 1394a, 3.4.1, Self-Identification Packet, ID packet is a special packet different from a normal packet and using during a self-ID phase of arbitration. In contrast to Ikegawa and the IEEE standard 1394, the claimed present invention determines whether there is an error in detection data on a bus and information including ID packets received from respective nodes in a topology ***DURING*** a bust reset sequence, which initializes information related to the bus of all of the nodes in the topology, determines a route node, determines an exclusive ID number for each node, and notifies the ID numbers to every node in the topology, to determine whether the bus reset

sequence is being performed normally.

Therefore, in contrast to Ikegawa and the IEEE Standard 1394, the claimed present invention is drawn to the distinguishing features of FIGS. 4 and 8, as recited in independent claims 1, 2 and 32, using claim 1 as an example, as follows.

> 1. (CURRENTLY AMENDED) An interface connectable to a host controller and an external bus, and that performs a predetermined bus reset sequence on the external bus, in response to a bus reset generated by a plug and play function according to a change in a status of the external bus, according to a process comprising:
>
> ***analyzing bus reset sequence data***, including identification (ID) packet, provided from the external ~~bus~~bus, ***during*** the bus reset sequence ~~and~~,
>
> determining whether the bus reset sequence has been completed normally according to the analyzing of the bus reset sequence data, and
>
> ~~wherein the analysis circuit provides~~***providing*** the bus reset sequence data ***to the host controller*** when ~~determined that~~according to the determining the bus reset sequence has been completed ***normally*** (emphasis added).

Support for the claim amendments can be found, for example, on page 17, lines 7-30 of the present Application.

INDEPENDENT CLAIMS 13, 24 AND 33

Independent claims 13, 24, and 33, which are drawn to the claimed present invention's "self-diagnosis by an interface," are patentably distinguishing over Ikegawa, at least based upon the same rationale for allowability of independent claim 35 by providing "a self-diagnosis circuit performing ***self-diagnosis*** of the interface ***using data transferring between the transmitting and the receiving circuits*** of the interface ***prior*** to the predetermined ***connection*** procedure ***with the network***."

However, the Examiner in page 10 of the Office Action appears to assert that the IEEE 1394 bus reset is a form of self-diagnosis. Further, the Examiner asserts on page 11 of the Office Action, that in IEEE 1394 the ports/connectors in the physical layer must be first interconnected before any actual connection procedure (adding a new node, for example) so that data can be actually transmitted and received. However, in contrast to the IEEE 1394 standard, in the claimed present invention the self diagnosis is based upon data transferring ***between the transmitting and the receiving circuits of one device without using the network bus***, such as the IEEE 1394 bus in case of IEEE 1394 (page 27, lines 10-16, of the

present Application) (i.e., "self-diagnosis ... ***PRIOR*** to a the predetermined ***connection procedure with the network***," e.g., claim 13).

In contrast to Ikegawa, the present invention as recited in independent claims 13, 24 and 33, using claim 13 as an example provides:

> 13. (CURRENTLY AMENDED) An interface having a transmitting circuit and a receiving circuit, and that performs a predetermined connection procedure with a network, the interface comprising:
>
> a self-diagnosis circuit performing self-diagnosis of the interface using data transferring between the transmitting and the receiving circuits of the interface ***prior to the predetermined connection procedure with the network***,
>
> wherein the interface suspends transition to the predetermined connection procedure with the network, when the self-diagnosis circuit generates a diagnosis indicating an abnormality of the interface.

Further, in contrast to Ikegawa, independent claim 33, as amended for clarity, provides:

> 33. (CURRENTLY AMENDED) A method of self-diagnosis by an interface having a transmitting circuit and a receiving circuit that are communicably connectable to an external bus, and the interface performing a predetermined bus connection procedure to connect with the external bus, comprising:
>
> connecting the transmitting circuit and the receiving circuit to each other ***prior to ~~a~~ connecting with the external bus via the predetermined bus connection procedure by the interface to connect with the external bus***;
>
> ***transferring data from the transmitting circuit to the receiving circuit***;
>
> comparing ~~received~~ data received by the receiving circuit with the transferred data; and
>
> self-diagnosing the transmitting and the receiving circuits according to the comparing of the ~~received~~data transferred and the data received ~~transferred data~~ ***between the transmitting and the receiving circuits, respectively, of the interface***.

CONCLUSION

In view of the claim amendments and remarks, withdrawal of the rejections of pending claims and allowance of pending claims is requested.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Respectfully submitted,
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